AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Currently amended) A semiconductor device, comprising:

a semiconductor substrate having formed thereon a semiconductor element;

a first wiring layer formed on said semiconductor substrate above an operating region where said semiconductor element is formed, said first wiring layer being electrically connected to said operating region;

a second wiring layer formed on said semiconductor substrate above said first wiring layer; and

a bonding pad to be electrically connected to an external connection terminal, formed on said semiconductor substrate above said second wiring layer, at least a part of said bonding pad being located above said operating region,

wherein said second wiring layer includes a plurality of wirings formed in the region under said bonding pad, a predetermined wiring of said plurality of wirings is electrically connected to said bonding pad, and an insulating film is provided for insulating said bonding pad from other wirings than the predetermined wiring among said plurality of wirings so that a plurality of wirings of the second wiring layer, which are located directly under the bonding pad, are insulated from the bonding pad by the insulating film, wherein said insulating film is formed over said other wirings so as to directly contact the bonding pad;

said other wirings provided parallel to the edges of said bonding pad are not formed in regions right under the edges, and wherein at least one of said other wirings of said second wiring layer that is insulated from said bonding pad is electrically connected to the first wiring

layer by way of a via defined in an insulator located between said first and second wirings layers; and

said insulating film is made up of an inorganic insulating film only, so that no organic insulating film is provided between the other wirings and the bonding pad.

2. (Original) The semiconductor device as set forth in claim 1, wherein: said other wirings are not formed in expanded regions right under said expanded regions as expanded with a stress in a process of electrically connecting said bonding pad to an external connection terminal, said other wirings being provided parallel to the edges to be moved in an expanding direction of said expanded regions of said bonding pad.

3. (Original) The semiconductor device as set forth in claim 2, wherein: respective lengths of the expanded regions in the expanding direction of said bonding pad are set to fall in a range of from 2 μm to 3 μm.

4. (Original) The semiconductor device as set forth in claim 2, wherein: said bonding pad and said external connection terminal are electrically connected by the chip-on-glass.

5. (Original) The semiconductor device as set forth in claim 2, wherein: said bonding pad and said external connection terminal are electrically connected by the chip-on-board.

6. (Previously presented) The semiconductor device as set forth in claim 1, wherein:

said bonding pad is to be electrically connected to an ~~said~~ inner lead by an inner lead bonding process, and

said other wirings formed parallel to the edges of a region to be electrically connected to said inner lead on a surface of said bonding pad are not formed in regions right under the edges.

7. (Currently amended) A semiconductor device, comprising:

a semiconductor substrate having formed thereon a semiconductor element;

a first wiring layer formed on said semiconductor substrate at above an operating region where said semiconductor element is formed, said first wiring layer being electrically connected to said operating region;

a second wiring layer formed on said semiconductor substrate at above said first wiring layer; and

a bonding pad to be electrically connected to an inner lead by an inner lead bonding process, formed on said semiconductor substrate at above said second wiring layer, at least a part of said bonding pad being located right above said operating region,

wherein said second wiring layer includes a plurality of wirings formed in the region right under said bonding pad, a predetermined wiring of said plurality of wirings is connected to said bonding pad, and an insulating film is provided for insulating said bonding pad from other wirings than the predetermined wiring among said plurality of wirings so that a plurality of wirings of the second wiring layer, which are located directly under the bonding pad, are insulated from the bonding pad by the insulating film, and wherein said insulating film is formed over said other wirings so as to directly contact the bonding pad;

said other wirings provided parallel to edges of said bonding pad are not formed in regions right under the edges of the regions electrically connected to the inner lead on the surface of said bonding pad, and wherein at least one of said other wirings of said second wiring layer that is insulated from said bonding pad is electrically connected to the first wiring layer by way of a via defined in an insulator located between said first and second wirings layers; and

said insulating film comprises an inorganic insulating film only, so that a bottom surface of the bonding pad does not contact any organic insulating film.

8. (Original) The semiconductor device as set forth in claim 6, wherein: said other wirings are not formed in expanded regions right under said expanded regions as expanded with a stress in the inner lead bonding process, said other wirings being provided parallel to the edges to be moved in an expanding direction of said expanded regions of said bonding pad.

9. (Original) The semiconductor device as set forth in claim 8, wherein: the respective lengths of the expanded regions in the expanding direction of said bonding pad fall in a range of from 2 μm to 3 μm.

10. (Previously presented) The semiconductor device as set forth in claim 1, wherein: said insulating film is made up of a silicone oxide film and a silicone nitride film, formed by CVD.

11. (Currently amended) A semiconductor device, comprising:

a semiconductor substrate having formed thereon a semiconductor element;

a first wiring layer formed on said semiconductor substrate at above an operating region where said semiconductor element is formed, said first wiring layer being electrically connected to said operating region;

a second wiring layer formed on said semiconductor substrate at above said first wiring layer; and

a bonding pad to be electrically connected to an external connection terminal, formed on said semiconductor substrate at above said second wiring layer , at least a part of said bonding pad being located right above said operating region,

wherein said second wiring layer includes a plurality of wirings, a predetermined wiring of said plurality of wirings is connected to said bonding pad, and an insulating film is provided for insulating said bonding pad from other wirings than the predetermined wiring among said plurality of wirings so that a plurality of wirings of the second wiring layer which are located directly under the bonding pad are insulated from the bonding pad by the insulating film, and wherein said insulating film is formed above said other wirings so as to directly contact the bonding pad;

said other wirings are formed so as to avoid regions right under the edges in the lengthwise direction of said bonding pad to 3 μm outside the regions, and wherein at least one of said other wirings of said second wiring layer that is insulated from said bonding pad is electrically connected to the first wiring layer by way of a via defined in an insulator located between said first and second wirings layers; and

said insulating film includes an inorganic insulating film, so that no organic insulating film is provided between the other wirings and the bonding pad.

12. (Original) The semiconductor device as set forth in claim 11, wherein: said insulating film is made up of an inorganic insulating film only.

13. (Original) The semiconductor device as set forth in claim 11, wherein: at least a part of said other wirings is formed in a region right under said bonding pad, and other wirings formed in the region right under the bonding pad are formed only in a region right under a region electrically connected to an inner lead on a surface of said bonding pad.